BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

REMARKS

Reconsideration of this application is respectfully requested. The objections to the claims have been overcome by making the changes suggested in the Action.

The rejection of claims 14, 15, 22, 25 and 26 as being anticipated by Narui et al (US Patent No. 6,150,689 - Narui) is traversed. Narui does not disclose a pad metal for an electrode pad covering an underlying active element.

The claims recite a pad metal for an electrode pad arranged over an active element, metal wiring layer, interlayer insulating film and barrier metal layer. Forming an electrode pad over an active element efficiently utilizes the semiconductor area under the pad. In the past, the area under an electrode pad had not been used for active elements. Application, page 4.

A pad metal (e.g., 14 in Figure 1) of an electrode pad provides a terminal for an external connection to the semiconductor device. As described in this application, the pad metal provides, for example, a terminal for bonding a wire to the semiconductor device. See Appln. pp. 20, 23, 32 and 45. The independent claims have been amended to make clear that the pad metal is for an electrode pad that forms "an external electrical terminal to said semiconductor device".

The claims recite an interlayer insulating film, e.g., 10a, 10b and 10c in Fig. 1 and films 42 and 43 in Fig. 15, between an active element and the pad metal. Independent claims 14 and 15 only require one interlayer insulating film. Independent claims 22 and

25 recite a plurality of interlayer insulating films, such as films 42 (40 a-e) and 43 (40 a-e) shown in Figure 15. The interlayer insulating film includes a level compensating film, e.g., the spin-on-glass (SOG) layer 10b and 40d. See e.g., pp. 17, 28, 35, 49 and 52. In the context of independent claims 22 and 25, the level of difference compensating film is formed below an uppermost metal wiring layer, and is formed between metal wiring layers (see page 30, line 24 to page 31, line 23 of the specification and Figs. 5-8, 10, and 14-18).

New claims 28 to 31 recite a "through hole" in the interlayer insulating film. The through-hole does not penetrate the level compensation film, e.g., soft film. Narui does not teach a through hole in an interlayer insulating film that does not penetrate the compensation film.

The objective of Narui is to simplify a manufacturing process by commonly carrying out the step of forming an electrode of an information storage capacitor and the step of forming metallic interconnection of a peripheral circuit. Narui does not tackle the problems addressed by the present application at all. Particularly, Narui does not suggest a compact architecture for a semiconductor device having a pad metal.

The Action improperly states that wiring layer 41B in Narui is a pad metal. The internal wiring select line (41B) of the memory circuit shown in Narui (Figs. 54, 55 and 61) is not a pad metal. See Narui, col. 16, lns. 19-23 and Fig. 3. Contrary to the Action, wiring layer 41B is disclosed in Narui as:

> **A Y select line YS and second interconnection layers 41A, 41B of the peripheral circuit are, respectively, formed on**

the silicon oxide film 40 as shown. The interconnection 41A is electrically connected to the plate electrode 35 via a connection hole 42 made at the insulating films (i.e. the silicon oxide film 40, the SOG film 39 and the silicon oxide film 28) which have been formed on the plate electrode 35 of the capacitor C, by which a plate potential ($v_{dd/2}$: a potential corresponding to a half of an applied voltage V_{dd} from outside of the semiconductor chip) is supplied to the plate electrode 35. **The interconnection 41B is electrically connected to the interconnection 30B via a connection hole 43 made at the insulating films (i.e. the silicon oxide film 40, the SOG film 39, the silicon oxide film 38, the silicon oxide film 32, the SOG film 31 and the silicon nitride film 27) which have been formed over the first interconnection layer 30B of the peripheral circuit**. A tungsten (W) plug 44 is embedded in the inside of the connection hole 42 for connection between the interconnection 41A and the plate electrode 35 and also in the connection hole 43 for connection between the interconnection 41B and the interconnection 30B, respectively. **The Y select line YS and the interconnections 41A, 41B are each made of a conductor film** whose sheet resistance is smaller than those conductor films for the gate electrode 8A (word line WL) and the gate electrodes 8B, 8C and also for the bit lines BL.sub.1, BL_2 and the interconnections 30A, 30B. For instance, such a conductor film is constituted of a three-layer conductor film wherein a TiN film an Al (aluminum) alloy film containing Si (silicon) and Cu (copper), and a TiN film are built up in this order. [Narui, col. 11, lns. 10-43 (emphasis supplied)]

Thereafter, a Y select line YS and second interconnection layers 41A, 41B are formed on the silicon oxide film 40, thereby approximately completing the DRAM shown in FIG. 3. **The Y select line YS and the interconnections 41A, 41B are, respectively, formed simultaneously by depositing a TiN film, an Al alloy film and a TiN film on the silicon oxide film 40 by sputtering, and patterning these films by etching through a photoresist mask.** The Y select line YS and the interconnections 41A, 41B may be formed of a built-up film of a TiN film and a Cu film, respectively. [Narui, col. 16, lns. 19-28 (emphasis supplied)]

The Y select line 41B disclosed in Narui is not a pad metal for an electrode pad nor an external electrical terminal. While the memory device that is the subject of Narui may have an associated electrode pad, it is not the Y select line nor is it described in the patent. There is no anticipation because Narui does not disclose a pad metal for an electrode pad.

Narui, (at column 11, lines 10-52 and particular at column 11, lines 43-52) describes that on a Y select line YS and interconnections 41A and 41B, an interconnection layer is disposed with an insulating film intervening therebetween, and a passivation film is further formed on the interconnection layer with another insulating film intervening therebetween. This indicates that the interconnection 41B in Narui is merely a part of the interconnections of the peripheral circuit, and thus not constituting an electrode pad which is an external electric terminal.

Narui does not include either one of the following arrangements: (i) only a portion of a level difference compensating film (SOG film) 31, 39 of an interlayer insulating film (27, 31, 32 or 38, 39, 40) covering an active element, the portion being under a pad metal, is removed and (ii) the level difference compensating film formed to a minimum thickness necessary for compensating the level difference of a metal wiring layer, e.g., the level difference compensating film is not formed on the uppermost metal wiring layer but only formed between the metal wiring layers.

Thus, an interconnection 41B of Narui is connected to an interconnection 30B, 35B via through-hole 43 made at an SOG film 31, 39. In contrast, the present application

describes the above-mentioned arrangements (i) and (ii) so that as in Figs. 5-8, 10, and 14-18, as a through-hole for connecting the pad metal with metal wiring layer and a through-hole for connecting the metal wiring layers with each other are formed so as not to penetrate the level difference compensating film.

Narui does not include a level difference compensating film formed to a minimum thickness necessary to compensate for the level difference of a metal wiring layer.

It appears that the rejection applies layer 31 in Narui as the level compensating film. This layer is thick and is contrary to the claim limitation for minimum thickness.

With respect to claim 22, Narui does not disclose "a lower interlayer insulating film **formed so as to cover said active element**". The Action identifies layers 17, 18, 19 of Narui (Fig. 54, 55 and 61) as corresponding to the claimed lower interlayer insulating film. Layers 17, 18 and 19 of Narui do not cover the diffusion layers 15 of the active element, as is required by claim 22. Similarly, Narui does not disclose a plurality of multilayer interlayer insulating films, as is required by claim 25.

The rejection of dependent claim 16 and 27 as being obvious over Narui in view of Hosomi et al (US Patent No. 5,773,888) is traversed for at least the same reasons stated above with respect to claim 14, on which depend claims 16 and 27.

Further, the passivation film (3) disclosed in Hosomi is applied outside the context of the present invention involving layers over an active element having insulating films, metal wiring layers, and a pad metal. Moreover, there is no suggestion to combine the Hosomi passivation film with the semiconductor memory structure shown in Narui

because Narui does not relate to pad metals or the stresses caused when bonding to pads, and Hosomi et al do not suggest that stresses induced by bonding may be alleviated by a passivation film that covers a large portion of a pad metal. It would not have been obvious to apply Hosomi et al to modify the semiconductor device disclosed in Narui in order to form the claimed invention.

All claims are in good condition for allowance. If any small matter remains outstanding, the Examiner is requested to telephone applicants' attorney. Prompt reconsideration and allowance of this application would be appreciated.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: _____

Jeffry H. Nelson
Reg. No. 30,481

JHN:maw
1100 North Glebe Road, 8th Floor
Arlington, VA 22201-4714
Telephone: (703) 816-4000
Facsimile: (703) 816-4100